Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDL5V0B20P1M5 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

TESDL5V0B20P1M5 is a unique design which includes proprietary clamping cells in a small package.

During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDL5V0B20P1M5 may be used to provide ESD protection up to ±30kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 6A (8/20μs) according to IEC61000-4-5.

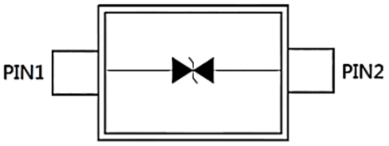
FEATURES

- ESD protect for 1 line with bidirectional
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC 61000-4-5 (Lightning) 6A (8/20us)
- Suitable for 5V and below, operating voltage applications
- Small package saves board space
- Protect one I/O line or one power line
- Fast response time
- Low leakage
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- Computers and peripherals
- Power supply protection
- Portable devices
- Audio and video equipment
- Notebooks, desktops, and servers

Pb-Free RoHS COMPLIANT HALOGEN FREE

PACKAGE: SOD-523F	PIN CONFIGURATION		CIRCUIT DIAGRAM
			
	PIN 1	Anode 1	
	PIN 2	Anode 2	

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Peak pulse power (tp = 8/20us)	P_{PK}	84	W
Peak pulse current (tp = 8/20us)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Operating junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	6	-	-	V
Reverse leakage current	V_{RWM} = 5V, T_J = 25°C	I_R	-	-	100	nA
Clamping voltage(1)	I_{PP} = 1A, tp = 8/20us	V_C	-	-	9.0	V
	I_{PP} = 3A, tp = 8/20us		-	-	10.7	V
	I_{PP} = 5A, tp = 8/20us		-	-	13.5	V
	I_{PP} = 6A, tp = 8/20us		-	-	14.0	V
Clamping voltage(2)	I_{TLP} = 16A, tp = 100ns	V_{CL}	-	12	-	V
Junction capacitance	1MHz, V_R = 0V	C_J	-	12.7	20	pF
Dynamic resistance(2)		R_{DYN}	-	0.3	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. RDYN is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDL5V0B20P1M5 RKG	SOD-523F	3,000 / 7” Tape & Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

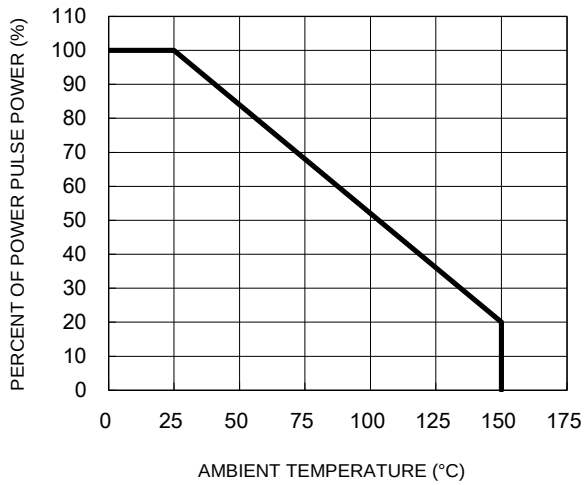


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

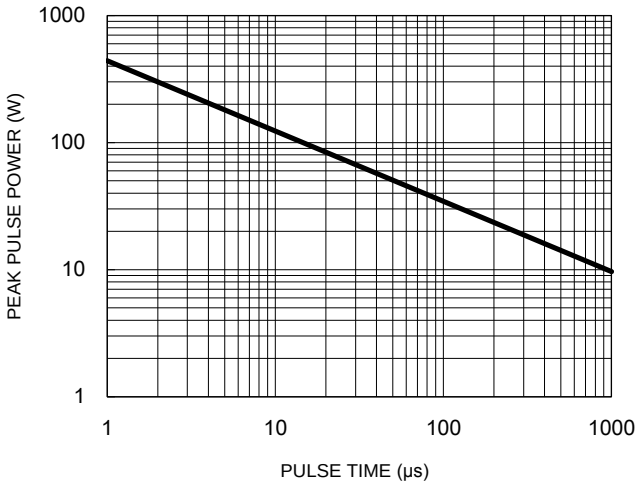


Fig.3 Clamping Voltage vs. Peak Pulse Current

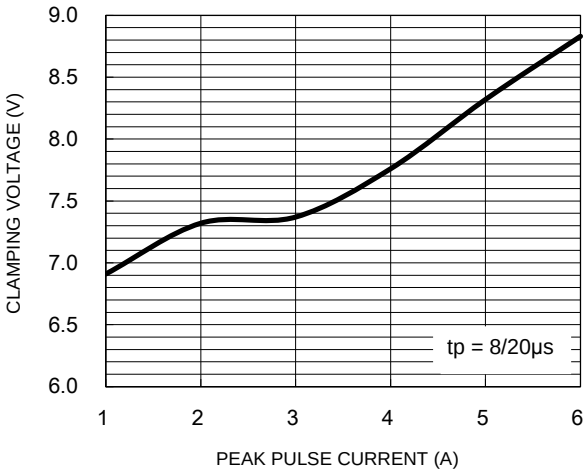


Fig.4 Capacitance vs. Reverse Voltage

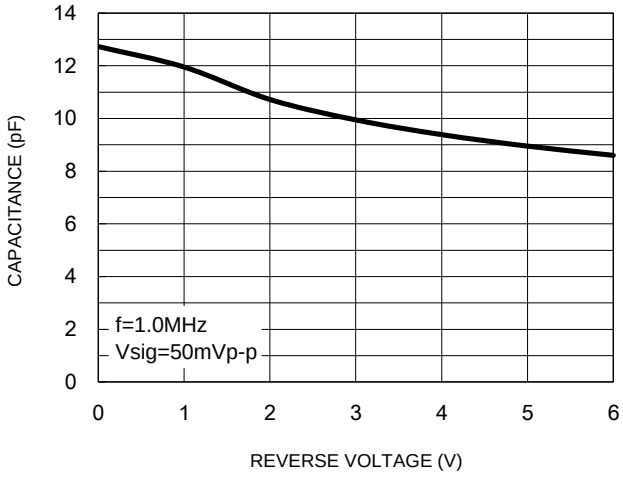
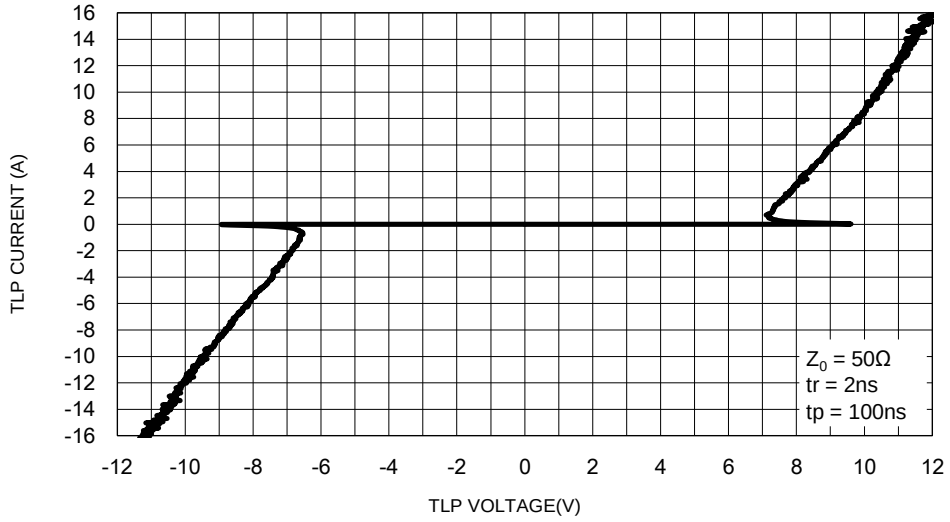


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform

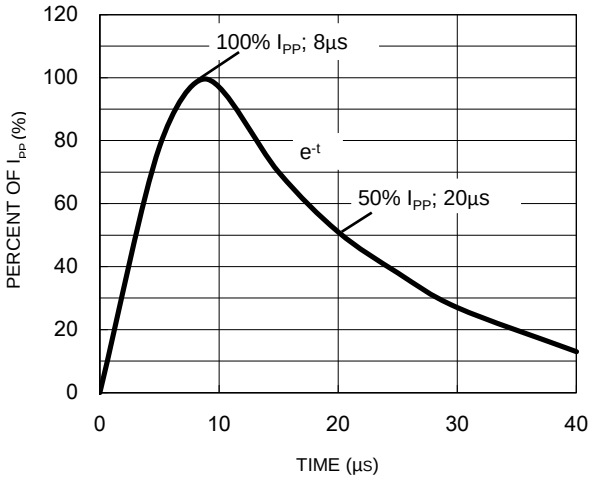
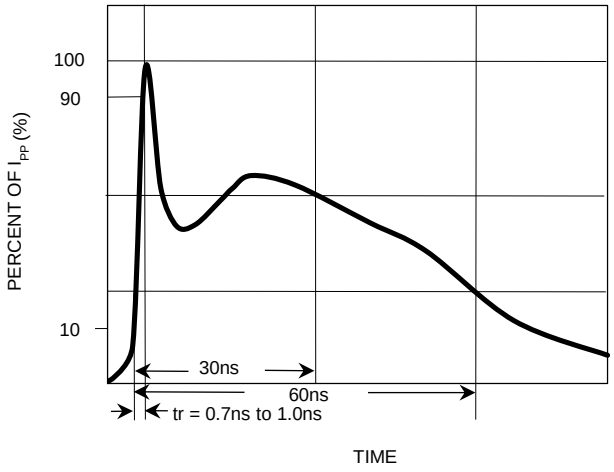


Fig.7 ESD pulse waveform



APPLICATION INFORMATION

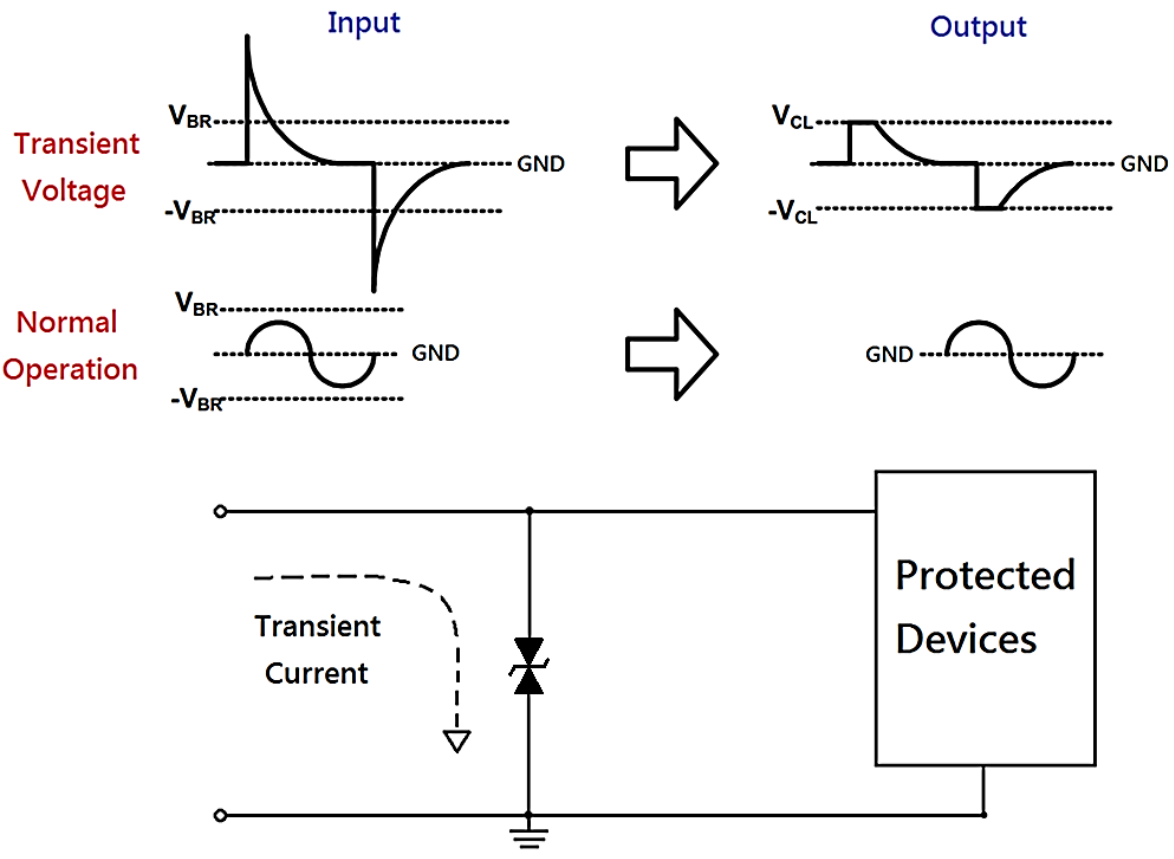
Device Connection

The TESDL5V0B20P1M5 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.
The usage of the TESDL5V0B20P1M5 is shown in Fig1.Protected line, such as data line, control line, or power line. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDL5V0B20P1M5 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

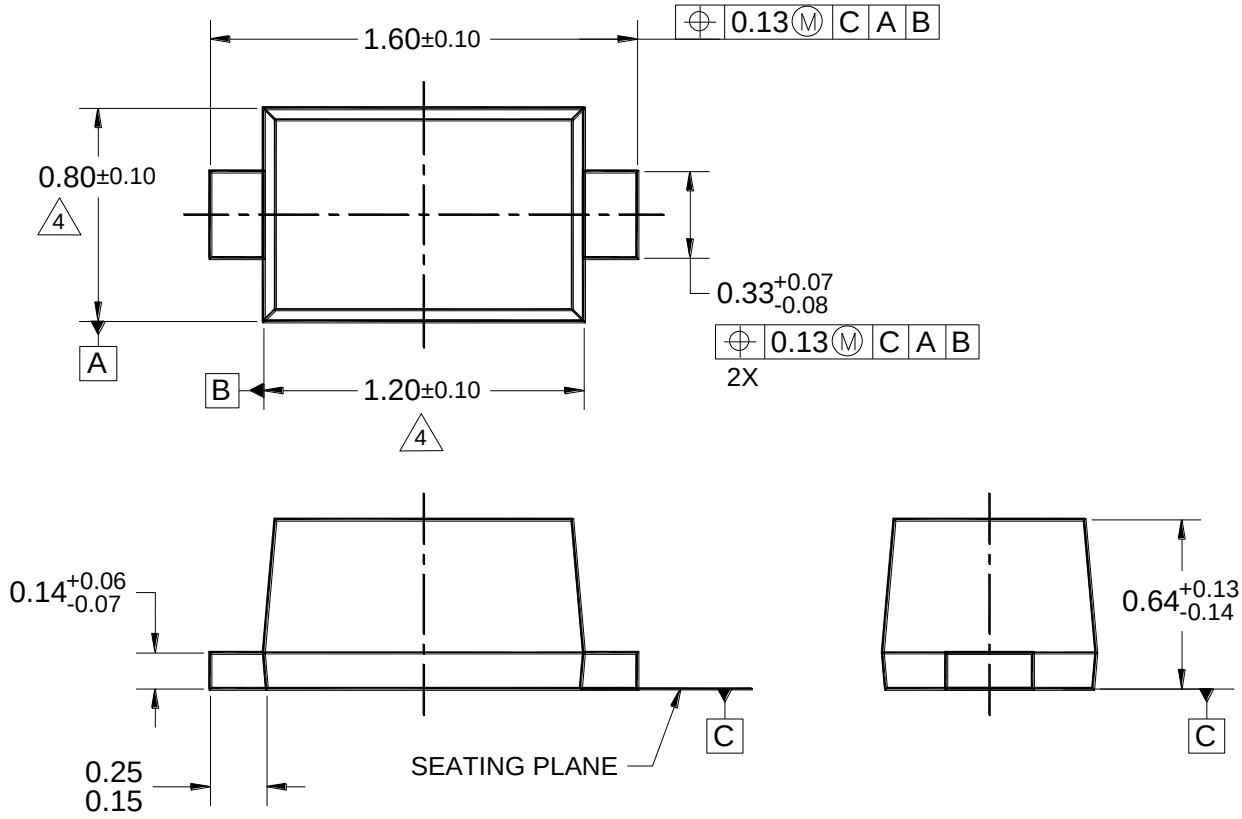
- Let the path length between the protected lines and the TESDL5V0B20P1M5 minimize.
- Place the TESDL5V0B20P1M5 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

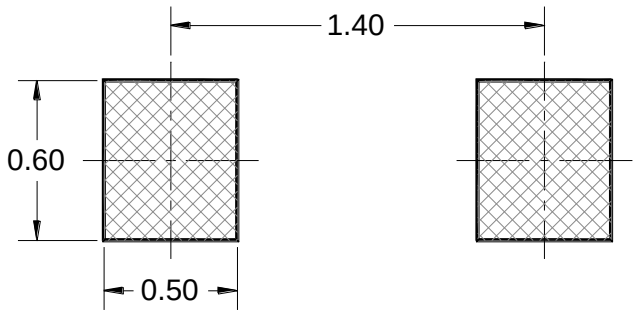
Fig.1 ESD protection by TESDL5V0B20P1M5



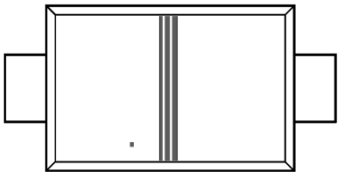
PACKAGE OUTLINE DIMENSIONS

SOD-523F





SUGGESTED PAD LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: EIAJ ED-7500A, SC-79.
4. MOLDED PLASTIC BODY LATERAL DIMENSIONS DO NOT INCLUDE MOLD FLASH.
5. DWG NO. REF: HQ2SD07-SOD523F-047 REV A.